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Response Under 37 C.F.R. § 1.116
Expedited Procedure
Examining Group: 2811

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Shreesh Narasimha, et al.	**Examiner:**	Quang D. Vu
Serial No.:	10/763,308	**Art Unit:**	2811
Filed:	January 23, 2004	**Docket:**	FIS920020200US2 (16106A)
Dated:	February 8, 2005		

For: CMOS DEVICE INTEGRATION FOR LOW EXTERNAL RESISTANCE

Entered w/RCE 3-16-05

Confirmation No.: 6529

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Commissioner for Patents
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RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

In response to the Office Action dated December 14, 2004, applicants submit the following amendments and remarks for entry of record in the above-identified patent application.

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Dated: February 8, 2005

Leslie S. Szivos, Ph.D.